

The Wide Field Imager for the International X-ray Observatory

Lothar Strüder^{1,3}, Peter Lechner^{2,3} on behalf of the IXO-WFI consortium

1) Max-Planck-Institut für extraterrestrische Physik, 2) PNSensor GmbH, 3) MPI Halbleiterlabor

Introduction

Since May 2008 the International X-ray Observatory (IXO) mission is under assessment as a joint European-Japanese-American unified vision of the previously independent projects XEUS and Constellation-X with an intended launch date around 2020. IXO aims to study the high-energy universe with unprecedented sensitivity using large-area, high-resolution X-ray optics on a deployable optical bench and interchangeable complementary sensor systems. The focal plane instrumentation includes a micro-calorimeter, a wide field imager, a grating spectrometer, a hard X-ray camera, a high time resolution spectrometer, and an X-ray polarimeter. For the Wide Field Imager (WFI) the X-ray optics with large collecting area and good angular resolution, the wide bandwidth, the required high radiation tolerance and high-speed flexible readout have stimulated the development of a new detector. The baseline WFI option is a monolithic, back-illuminated silicon Active Pixel Sensor based on the integrated detector-amplifier structure DePFET which unifies the science driven specifications in one device. A first series of prototype devices is in compliance with the IXO specifications.

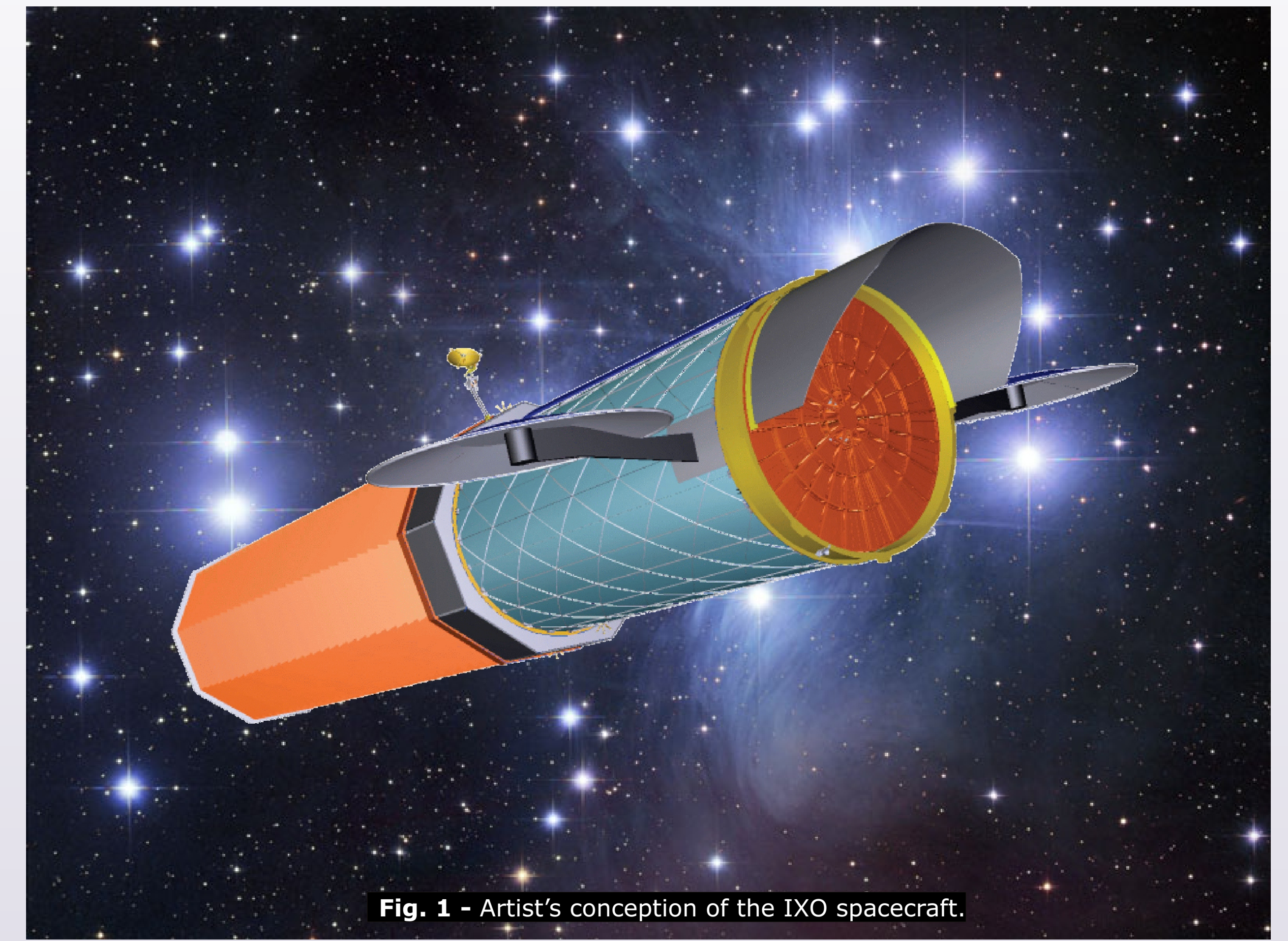


Fig. 1 - Artist's conception of the IXO spacecraft.

The DePFET principle

The DePFET (**D**epleted **P**-channel **F**ield **E**ffect **T**ransistor) is an integrated detector-amplifier device. It consists of a p-channel FET on a n-type bulk that is fully depleted by a reverse biased backside diode. The applied voltages and deep implantations generate a local potential minimum for electrons underneath the transistor channel. Signal electrons are collected in this 'internal gate' and modulate the transistor current by inducing positive image charges in the p-channel, and the FET current is a function of the energy absorbed in the depleted volume.

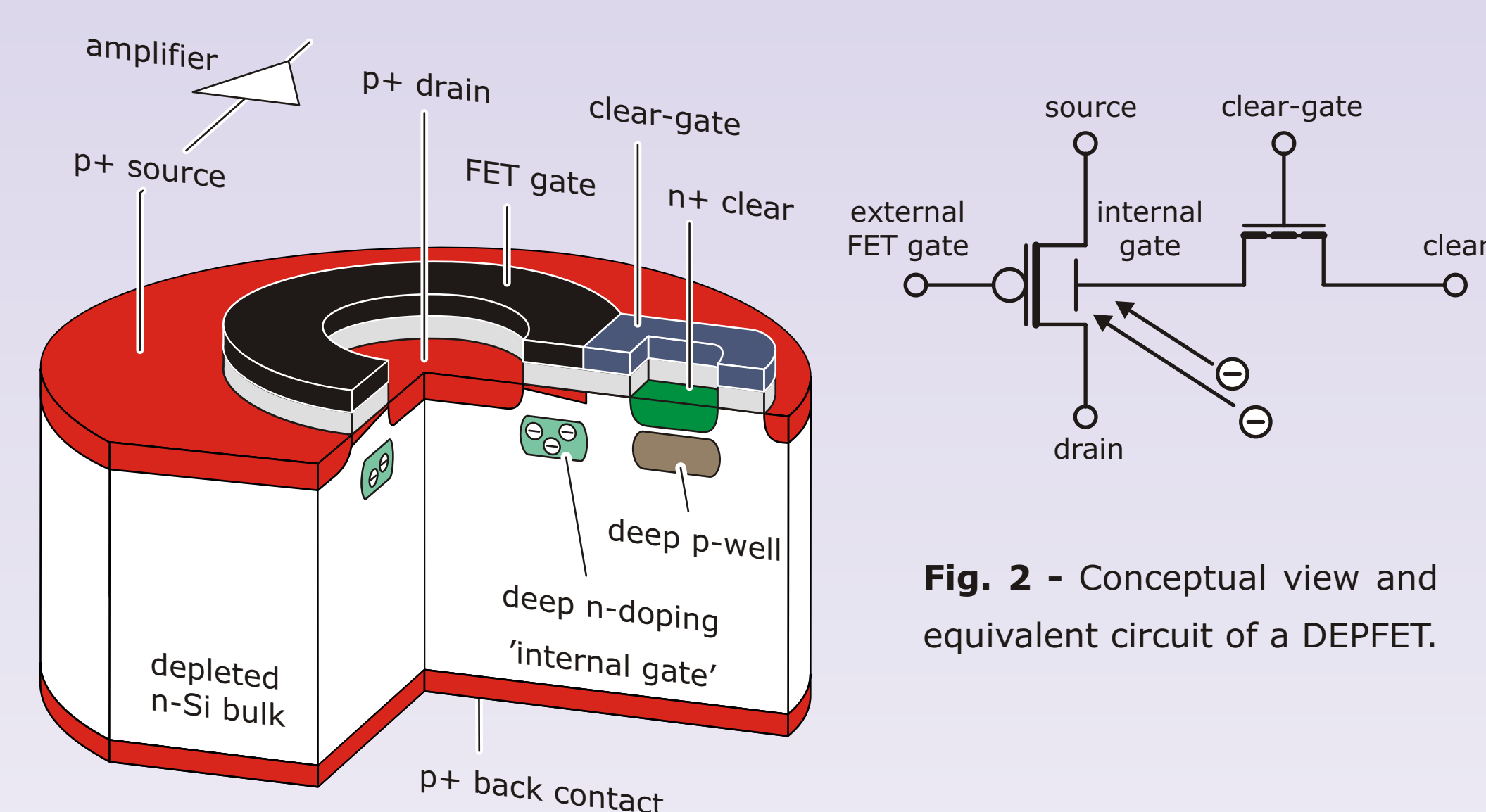


Fig. 2 - Conceptual view and equivalent circuit of a DePFET.

Periodic clocking of the adjacent n-doped clear contact and clear-gate to a positive voltage resets the DePFET, the signal charges are removed from the internal gate.

The DePFET concept combines unique device properties:

- **internal amplification**
 - ▶ free of interconnection stray capacitances,
 - ▶ sensitivity of the internal gate $\Delta I = 300$ pA/electron,
- **analog signal storage**
 - ▶ signal collection in ON and OFF state,
 - ▶ readout on demand,
- **full depletion**
 - ▶ backside illumination,
 - ▶ high detection efficiency (450 μm Si, 97 / 35 % @ 10 / 20 keV).

The DePFET-based Active Pixel Sensor

The matrix arrangement of a number of DePFETs with common bulk and back contact results in an Active Pixel Sensor (APS) with

- **in-pixel signal storage and amplification,**
- **100 % fill factor,** no insensitive regions,
- back-illumination through a **homogeneous thin entrance window,**
- **scalable pixel size** from 30 μm \square to 1 cm^2 \square ,
- **low power,** as the DePFET is only turned on for readout,
- **random accessible pixels** allowing flexible readout modes:
 - ▶ sequential, CCD-like *full frame mode*,
 - ▶ *window mode* with free selectable regions of interest,
 - ▶ *mixed mode*, combined window & full frame mode,
 - ▶ *fast timing mode*, max. readout speed on a limited area with reduced energy resolution (e.g. 10^2 counts/sec, 16 x 16 pixels),

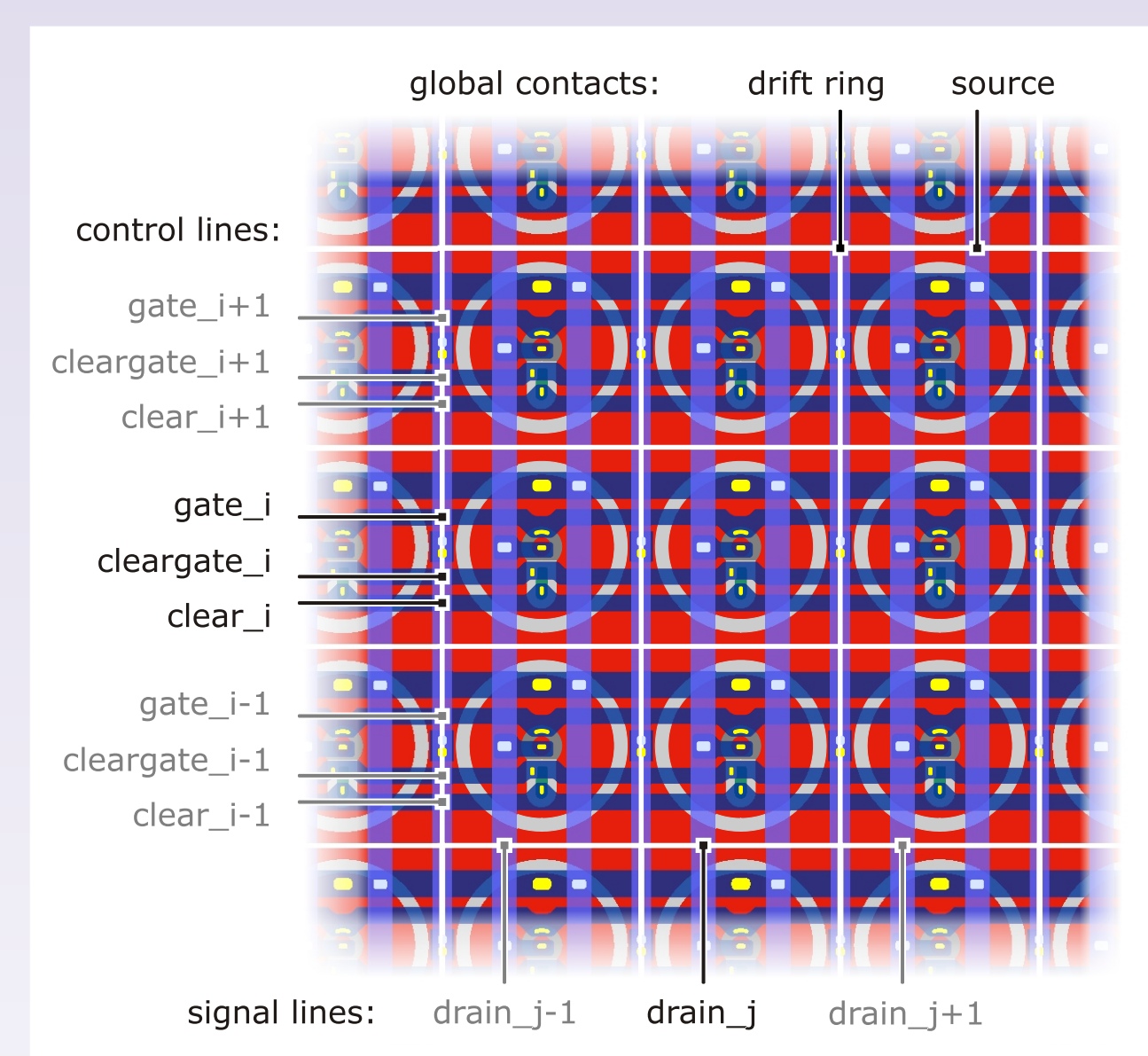


Fig. 3 - 3 x 3 pixel detail of the IXO-WFI tentative layout with a pixel format of 100 μm \square . For optimal signal charge collection and efficient area-filling the DePFETs have a circular shape and are surrounded by a drift ring structure focusing the signal electrons towards the pixel center.

- **column-parallel readout:**
 - ▶ row-wise connection of control contacts (gate, clear, clear-gate),
 - ▶ column-wise connection of readout nodes, i.e. drain contacts,
 - ▶ global contacts (source, drift ring, substrate, back contact),
- **cyclic readout:**
 - ▶ one active row with DePFETs turned on,
 - ▶ active row is scrolled cyclically through the pixel matrix,
 - ▶ other DePFETs turned off, still integrating signals,
 - ▶ integration time = (number of pixel rows) x (row processing time).

Frontend Electronics

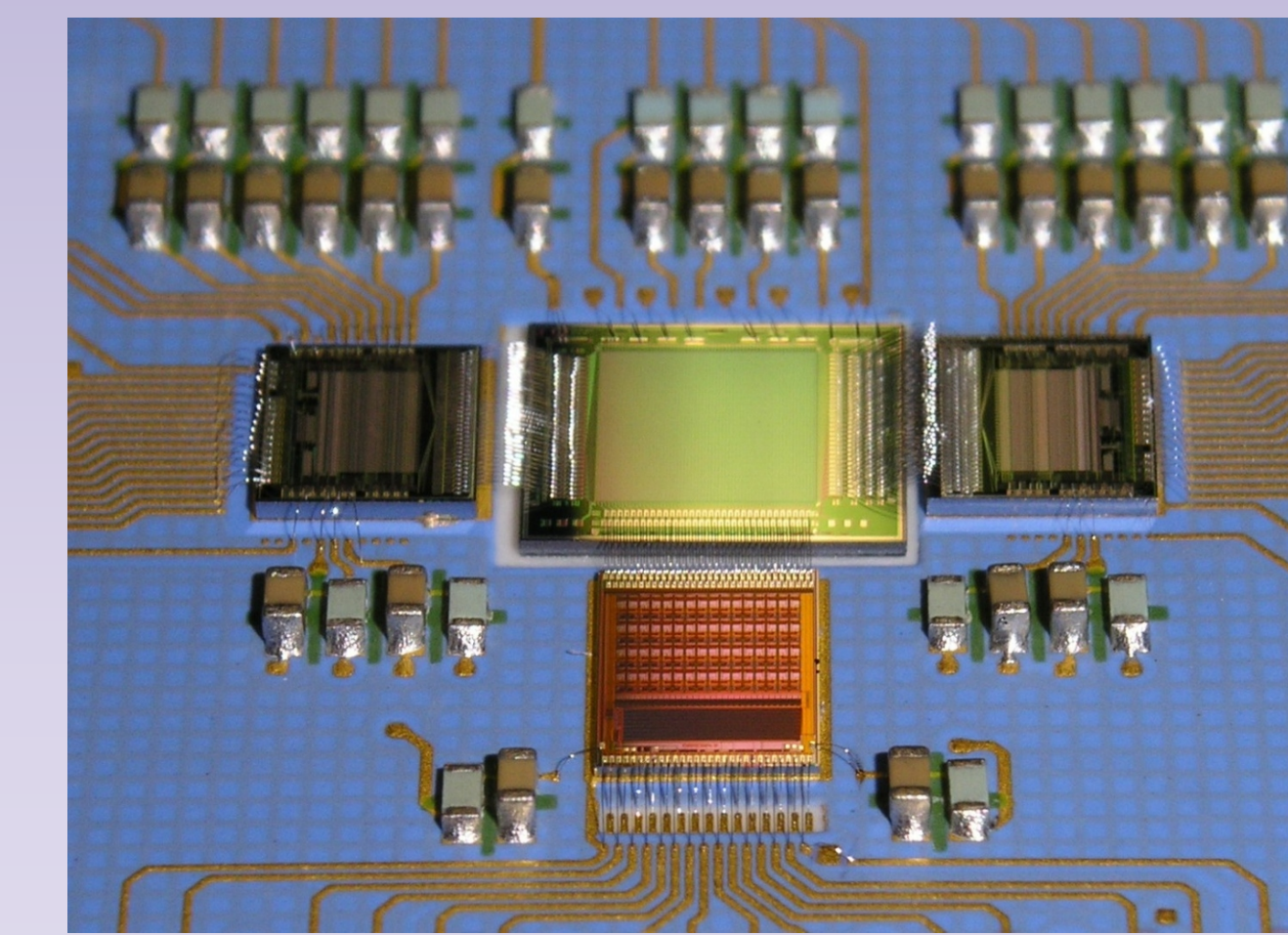


Fig. 4 - Prototype DePFET APS with 75 μm \square pixels and 64 x 64 format (middle), SWITCHER-II control chips (left and right), and VELA readout chip (bottom).

Readout sequence

A measurement of the DePFET current retrieves the signal information stored in the internal gate in a consecutive read-clear-read sequence:

1. first current measurement: baseline + signal
 2. reset, i.e. removal of signal charges by clocking clear and clear-gate,
 3. second current measurement: baseline.
- The signal amplitude is obtained from the current difference.

VELA readout chip (Politecnico di Milano)

- DePFET-specific development,
- 64-channel pre-amplifier & filter-amplifier, 64/1 analog multiplexer,
- current (de)integration filter with trapezoidal weighting function,
- high dynamic range by current subtraction circuit,
- fast readout: 2 μsec processing time per pixel row (and even below),
- tradeoff: readout speed vs. equivalent noise charge,
 - ▶ ENC = 4 el. @ 4 $\mu\text{sec}/\text{row}$,
 - ▶ ENC = 7 el. @ 2 $\mu\text{sec}/\text{row}$.

SWITCHER control chip

- DePFET-specific development,
- 64-channel dual-output switching circuit,
- supply of clocked analog voltages applied to gate, clear, clear-gate,
- high-voltage CMOS process, switching amplitude > 20 V,
- switching frequency > 20 MHz,
- daisy-chainable for the operation of large format APSs.

Prototypes

Prototype devices (fig. 4) with 64 x 64 pixels, 75 x 75 μm^2 pixel size, and 450 μm wafer thickness have been fabricated in a dedicated process technology including two poly-silicon layers and two metal layers and characterised at IXO-representative conditions at -60 °C with a readout speed of 2 μsec per pixel row.

Process quality

- leakage current level 10 fA/pixel @ RT (~ 100 pA/cm² @ RT),
- offset and gain variation < 3 %, noise dispersion < 10 %,
- no dead or bright pixels.

Spectral resolution

- $\Delta E = 126$ eV @ 4 $\mu\text{sec}/\text{row}$ (FWHM @ 5.9 keV, -60 °C),
- $\Delta E = 140$ eV @ 2 $\mu\text{sec}/\text{row}$ (FWHM @ 5.9 keV, -60 °C).

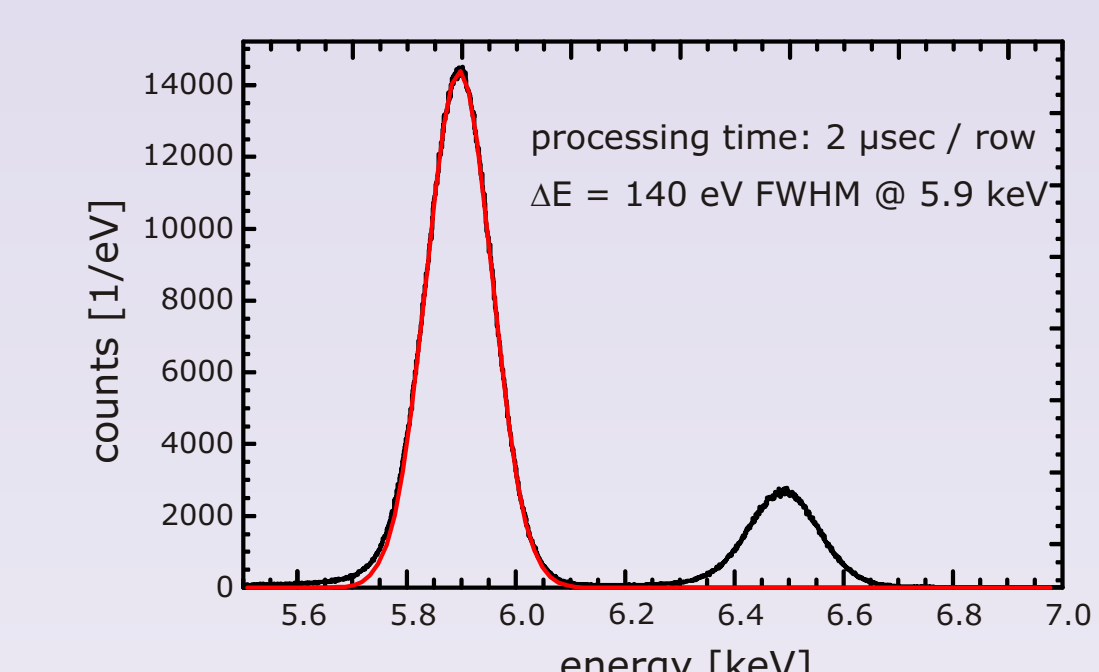


Fig. 5 - ⁵⁵Fe spectrum obtained with a 64 x 64 DePFET APS at -60 °C with VELA readout and fast processing time of 2 μsec per pixel row. The FWHM of the Mn-K α line is 140 eV.

Imaging

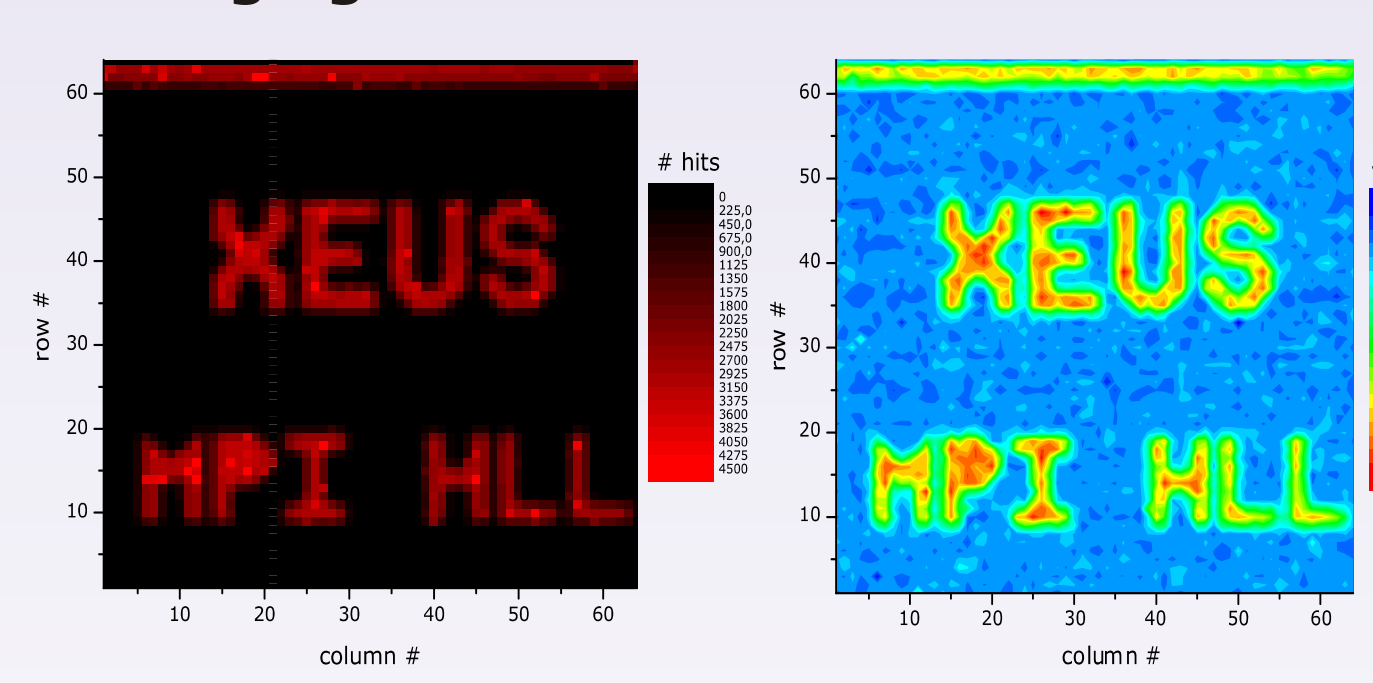


Fig. 6 - Shadow image of a Si mask: digital hit map (right), analog contour plot (left). The images contain 10^5 frames. The smallest feature size is 150 μm .

Radiation hardness

The DePFET is intrinsically radiation hard, as - unlike a CCD - there is no charge transport within the device. The leakage current generated by bulk damage is controlled through the operation temperature -60 °C and by the fast readout. Proton and X-ray irradiations have been performed:

- negligible leakage current @ 10^{10} p/cm² (10 MeV),
- tolerable threshold voltage shift < 1 V @ 10 krad.

The IXO Wide Field Imager

The specifications of the IXO Wide Field Imager are driven by top-level scientific and technical boundary conditions:

- **field of view (FoV) > 18 arcmin** (@ focal length 20 m)
 - ▶ sensor dimension > 10 x 10 cm^2 ,
 - ▶ 6' wafer-scale device with 'round' corners (fig. 7),
 - ▶ world's largest monolithic X-ray imaging & spectroscopy sensor,
 - ▶ FoV coverage: > 99.8 % @ 18 arcmin, > 90 % @ 20 arcmin,
- **angular resolution 5 arcsec** (= point spread function 500 μm HEW)
 - ▶ pixel size 100 x 100 μm^2 , 5 x oversampling of the HEW,
 - ▶ in total ~ 1 million pixels,
- **energy range 100 eV ... 15 keV**
 - ▶ ultra-thin radiation entrance window for low energies,
 - ▶ full depletion of 450 μm Si for high energies,
- **photon flux** (sampling area 3 m^2 @ 1.25 keV, 1 m^2 @ 6 keV)
 - ▶ column-parallel bi-directional readout, 2048 readout channels,
 - ▶ 2 μsec readout time per pixel row, full frame rate 1.000/sec,
- **raw data rate 2 GByte/sec**
 - ▶ efficient on-board data reduction algorithm required,
- **bright point source observation**
 - ▶ window mode with free selectable region of interest,
- **combination with hard energy X-ray camera**
 - ▶ monolithic device,
 - ▶ suspension mounting without mechanical support.

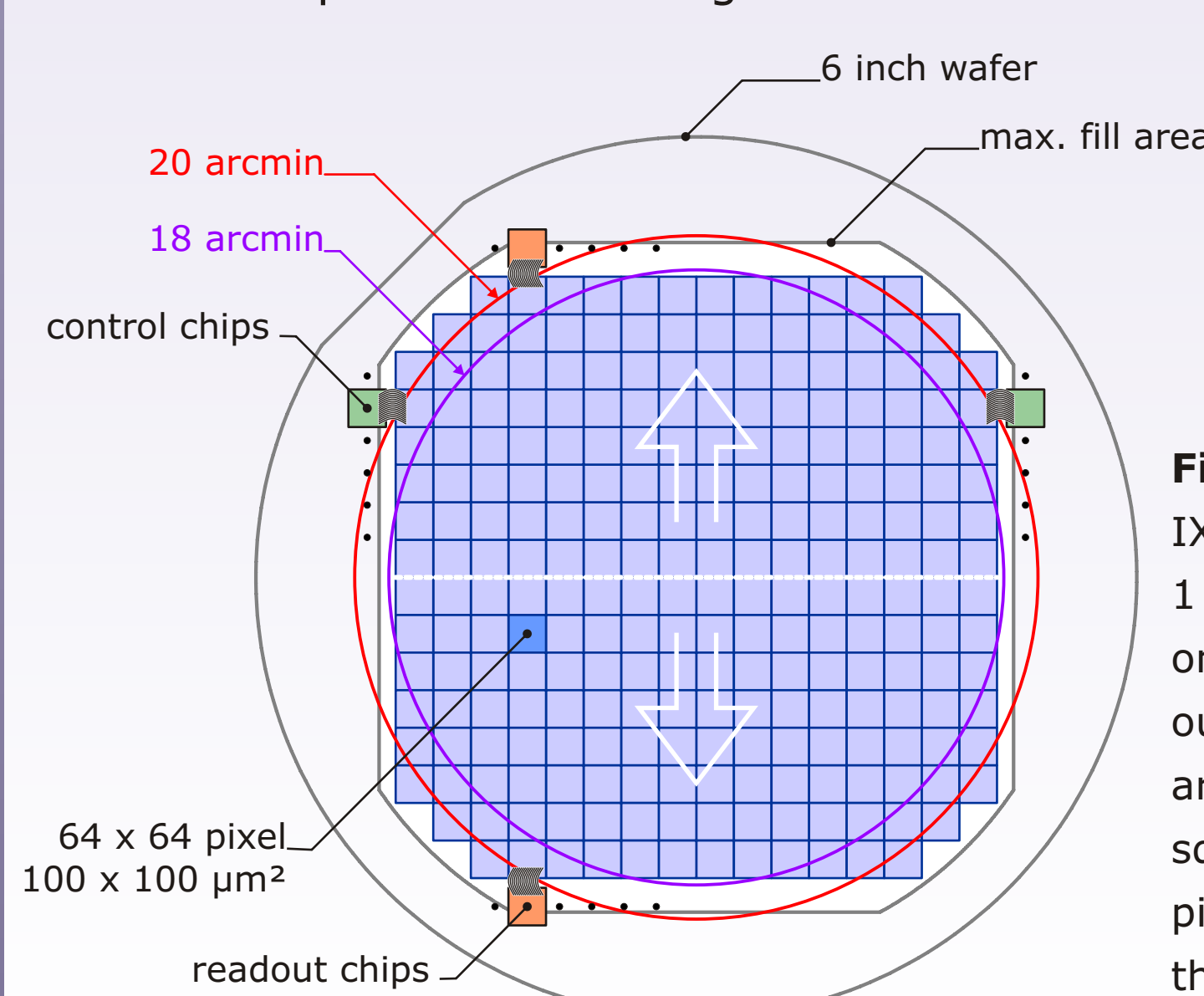


Fig. 7 - Tentative layout of the IXO-WFI focal plane detector with 1 million pixels of 100 μm size on a 6-inch silicon wafer. The outer dimensions of the sensitive area are 10.24 x 10.24 cm^2 . The squares are blocks of 64 x 64 pixels. The white arrows indicate the parallel bidirectional readout.

Next Steps

In a second production DePFET APS prototypes with representative large sensor formats have been processed (fig. 8):

- 75 μm \square pixels, 256 x 256 pixels, 1.92 x 1.92 cm^2 sensitive area,
 - 75 μm \square pixels, 128 x 512 pixels, 0.96 x 3.84 cm^2 sensitive area.
- Their characterisation is in preparation with the intention to demonstrate the homogeneity of large scale devices and the technology readiness of the DePFET approach for IXO.

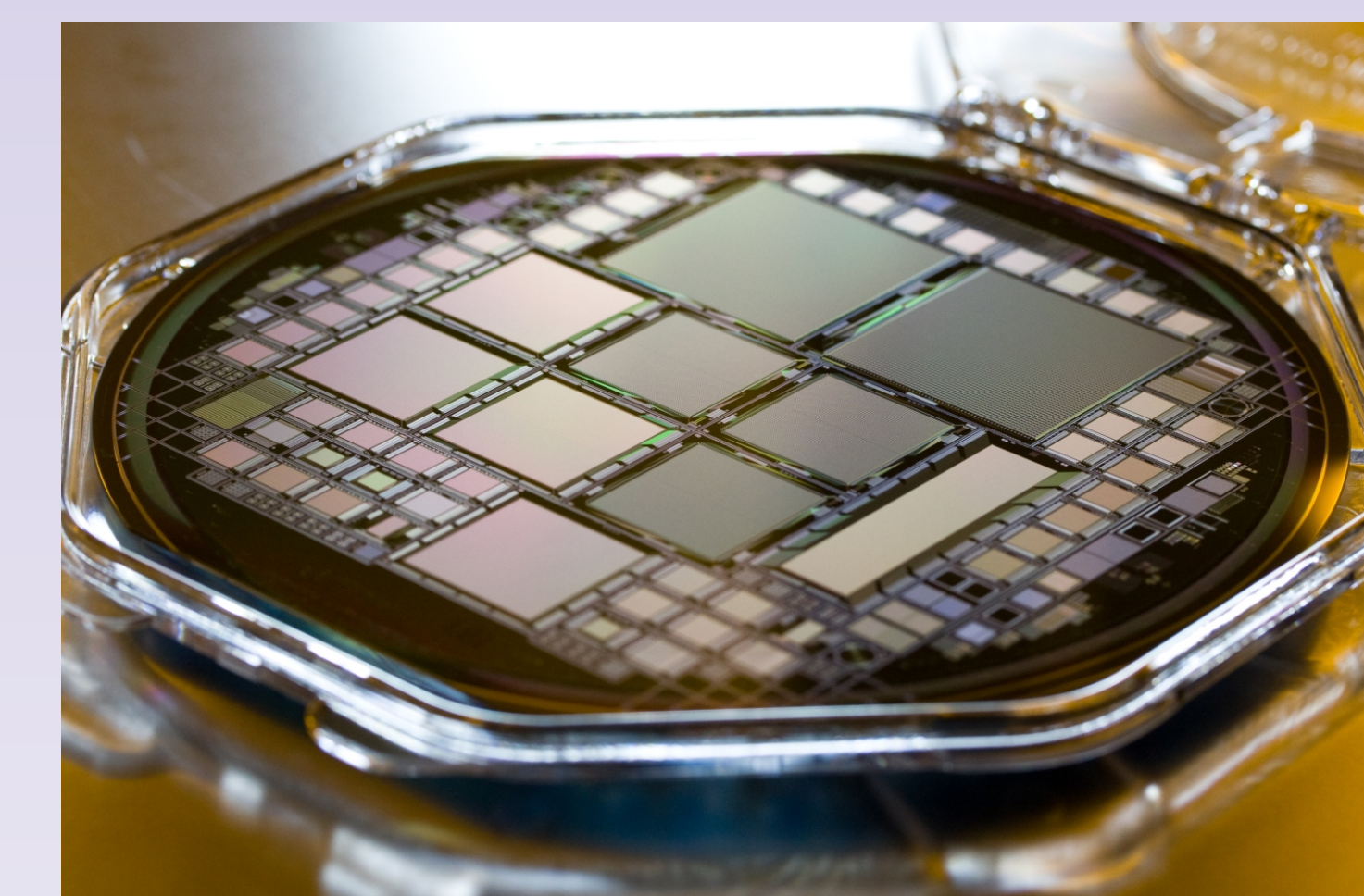


Fig. 8 - 6-inch Si wafer with APS prototypes for the IXO-WFI studies. The sensor formats are 256 x 256 pixels and 128 x 512 pixels with 75 μm \square pixel size.

Summary

- For the Wide Field Imager of the IXO mission we propose a wafer scale DePFET Active Pixel Sensor.
- The DePFET concept unifies the science driven top level requirements of IXO in one device.
- A dedicated process technology for the fabrication of DePFET APSs has been successfully applied in several prototype runs.
- A DePFET-specific frontend electronics system of readout and control chips has been developed.
- A laboratory data acquisition system scalable for the operation of large sensor formats has been installed.
- The concept of the sensor and frontend electronics has been proven by 64 x 64 prototypes with performance figures in accordance with the requirements of the IXO mission.
- A new generation of sensors with significantly larger formats is available for the demonstration of the DePFET technology readiness.